Electronic Packaging RF SiPs Demand Early Packaging Focus

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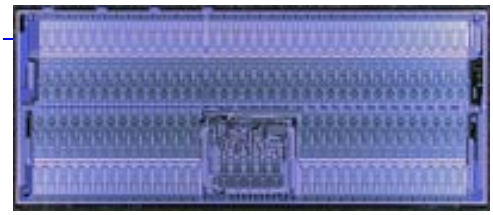

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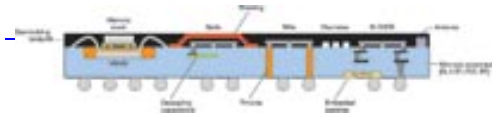
Wireless technologies have evolved swiftly over the past two decades. What were once large RF/microwave modules and monolithic microwave integrated circuits (MMICs) have become miniaturized, multi-function systems. Across the board, wireless products are smaller, more adaptable and higher performing than ever before. As a result, those developing cutting-edge RF applications are facing new opportunities — and also new challenges.

Medical innovators are working to develop RF functionality for pacemakers and other implantable devices. Aerospace and defense entities are creating new communication, surveillance and anti-jamming technologies for the modern battlefield. And industrial RF application developers are improving the real-time monitoring of field and factory operations.

While RF ASIC advancement continues, integrated circuit (IC) packaging is often an afterthought. This is increasingly problematic because packaging can impact the product development cycle and be a key factor in achieving an optimal price/performance ratio.

By considering packaging in the early stages of product development, design teams can determine the best architecture for their particular application. For example, designing an RF system-in-package (SiP) presents the opportunity to integrate antennas, baluns and filters into a single component solution. This can result in higher performance, lower cost and smaller footprint solutions relative to system-on-chip (SoC).

The Debate between SiP and SoC



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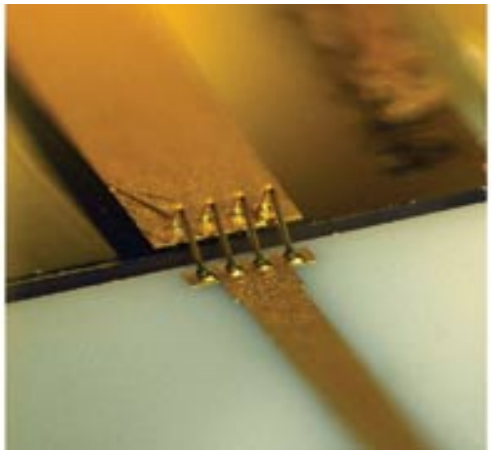
The choice between SiP and SoC often creates a lively debate among RF designers, primarily because neither offers a panacea for all applications. Both approaches deliver unique benefits and drawbacks. For instance, CMOS-based SoC may be an attractive approach for Bluetooth solutions. For high performance applications, however, it is often best to design the RF and analog functions into GaAs and SiGe, respectively. In many cases, the diversity of semiconductor technologies demands a flexible integration platform that time-tested CMOS technologies (e.g. 180 nm CMOS) cannot offer.

SiP allows for heterogeneous integration of specialized ASICs, which can enable re-use of RF, analog and digital ASICs across a diverse product portfolio. This can lead to reductions in product development lead-time and costs. And by maximizing the capabilities of analog, digital and RF ASICs within a single system, performance can be improved.

Just like the SoC model, SiP comes with its own hurdles. These include package design complexity; isolation of signal modalities (RF/analog/digital); accessibility of signals for module test; thermal management; creation of known good die; and fabrication of precision discretes in laminate SiP substrate technologies.

SoC-SiP Hybrid Solution

Although the SoC versus SiP debate continues, some development teams are finding that they can have the best of both worlds.



Because SoC represents an inherently rigid approach, design experts are now seeking to bring the power and size benefits of SoC to the SiP model. For example, the development of advanced CMOS nodes (e.g., 45 nm and 65 nm) has enabled the fabrication of mixed-signal (analog and digital) ASICs, which can be integrated

alongside an RF ASIC within a high performance package.

This type of SoC-SiP hybrid solution is becoming increasingly common. Besides the advancements in semiconductor processes, the proliferation of this approach can also be attributed to several enabling packaging technologies: die thinning and stacking; high-reliability flip chip technologies (e.g., low-stress underfills that are compatible with low-k ASICs); plated cavities in organic substrates to accommodate RF ASICs and/or RF MEMS; interconnect shaping (e.g., tuning wire-bond loop geometries, using gold stud bumps, and/or plastic core solder balls to achieve precision interconnect tolerances); development of low-loss, radiation-proof dielectrics with environmetally stable properties; quasi-hermetic packaging solutions that offer lower cost solutions over traditional ceramic implementations while providing sufficient moisture protection; embedded and laser-trimmed discretes; silicon substrates with through silicon vias (TSVs) and high-tolerance passives that can serve as an integration platform; and coreless organic substrates with stubless micro-via stacks.

All of these developments have reduced the size and cost of RF SiP solutions while improving performance. This, in turn, has made RF SiPs more attractive than ever, with lower non-recurring expenses (NREs), shorter development lead-times and tremendous design flexibility. These benefits can only be obtained, however, through a dedicated focus on advanced packaging in the early stages of product development — before architectural decisions have been made.

Contemporary Technologies

What package design will deliver the best power density? What material(s) will offer the least amount of stress or best thermal dissipation? How can the size and power consumption of the product be minimized? What is needed to ensure the reliability of the interconnections between the IC, the package and the rest of the system?

These are common considerations, but a focus on contemporary packaging technologies and advancements will help those developing high-performance RF applications to achieve price-performance goals.

Military Applications

Military and aerospace designers, for example, must consider the extreme conditions in which their applications will operate. Their devices require durability in harsh and spectrally chaotic operating environments where interference and jamming are prevalent, maintenance is out of the question and device uptime is a must.

Not surprisingly, these applications require reliable packaging solutions. Low-temperature co-fire ceramics have traditionally offered the best substrate solution in terms of passive integration, RF performance, hermeticity and chip-to-substrate interconnect reliability. However, liquid crystal polymer (LCP), with low-loss (≤3.0, ≤0.005) and low moisture absorption (≤.02%) characteristics, is a viable dielectric alternative for SiP substrates. A few substrate fabricators can offer this technology

in up to 4-layer configurations today, and by 2010, 8-layer stacks should become available. LCP has already been proven as a quasi-hermetic housing solution that can offer cost, weight and size improvements over kovar and ceramic. Today, LCP cannot offer the same interconnect densities and layer counts as coreless, PTFE (polytetrafluoroethylene) substrate solutions, however LCP holds promise, and is not susceptible to radiation damage like PTFE. This is because the process window for lamination of LCP plies is less than 5ºC and laser drilling processes have not been fine tuned for this particular material.

Medical Applications

Forthcoming implantable devices with wireless patient monitoring capabilities must also operate in a unique, albeit equally challenging, environment: the human body. Reliability is a concern, of course, and size plays a decisive role in the viability of implantable RF devices. Achieving low-volume, low-mass solutions typically implies use of a high-density interconnect organic substrate — with line widths of 15 to 20 µm and spacing of 20 µm, micro-via diameters of 50 µm on via pitches of less than or equal to 200 µm — to support routing of bumped, flip-chip die. Organic substrate technologies with these design rules are commercially available in both flex and rigid formats with embedded resistors (10 ohm to 5 kilo-ohm) and capacitors (5 to 25 nF/in^2) with untrimmed tolerances of ± 20% to support small form factor designs. Laser trimming of embedded passives (prior to lamination) can enhance these tolerances to ± 5%, but to achieve much tighter tolerances discrete solutions that are then attached to the surface of the SiP must be used.

RF designers working on implantable applications must also consider shielding of devices from noisy RF sources, such as interference from cellular phones. In these applications it makes sense to build cavities into a bio-compatible, magnetically-shielded housing for weight savings. To enable further size / weight reductions in the future, a molded, plastic SiP solution could be metallized to form a shielding layer and individual devices could be isolated in plated cavities within a SiP.

Recommendations

Regardless of industry or application, there are several recommendations for those working with modern RF ASICs and SiPs. As stated previously, consider packaging sooner rather than later. Early decisions concerning the ASIC's architecture and specifications may limit the ability to be flexible in designing the package as well as the overall effectiveness of the package solution.

Also, take advantage of proven, tested semiconductor technologies. Whereas SoC engineers often use the newest, most advanced (and least proven) CMOS nodes to achieve aggressive mixed-signal design requirements, SiP engineers developing high-reliability, high-performance RF products can use mature semiconductor processes in their designs. Known good building blocks, like 180 nm CMOS, reduce the risk of compromising project timelines and budgets.

Finally, seek advice and assistance from suppliers who specialize in advanced IC packaging. Those who have in-house engineering expertise, flexible assembly lines

and advanced testing capabilities go well beyond build-to-spec and contract manufacturing. They can develop robust design concepts and evaluate the trade-offs of each design alternative, and help guide product development teams through both known and unforeseen technology risks.

Conclusion

When it comes to modern RF applications, creating a high-performing ASIC is only half the challenge. An early focus on packaging will help RF designers and system architects better achieve their program objectives while reducing the risks inherent in any new product development project.

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