Low Cost FPGA-Based HD/SD SDI Transceivers

The recent advent of low-cost FPGAs equipped with high-performance transceivers and DSP blocks will greatly reduce the build and deployment costs of a video broadcast system.

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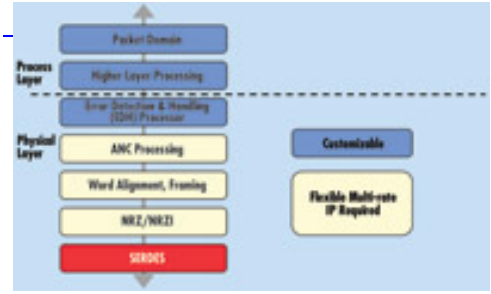

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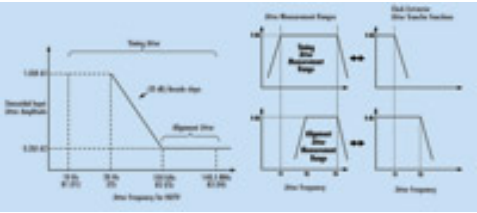
As the explosion of HDTV, IPTV, VoD and YouTube downloads continues, together with the increased capabilities and falling prices of FPGAs, it is inevitable that the two technologies will intertwine. A key part of the former is the ability to transmit, receive, edit and process uncompressed video. The transceiver portion of this requirement is served by the Society of Motion Picture and Television Engineers (SMPTE) through their Serial Digital Interface (SDI) family of standards. These standards define the physical interface and related circuitry needed to transport uncompressed digital video over 75Ω coax cable. If FPGAs are to be used in this market segment, it is essential that they comply with these standards. This article examines the benefits of and challenges faced by FPGA vendors in this regard.

Why FPGA-Based SMPTE Transceivers?

As in countless digital design applications, the FPGA fabric has always provided the system architect the ability to port the company's "secret sauce" in the FPGA fabric without having to resort to spinning a costly and time consuming ASIC. In the context of SMPTE-based systems, FPGAs deliver additional advantages.

Flexibility: FPGAs enable a single common design to be used across multiple platforms without the need to compromise the design in order to serve different markets, regional standards or performance targets.

Bridging: A single silicon platform will bridge SMPTE to multiple domains, be it the compressed transport domain (e.g. DVB-ASI), consumer space (e.g. DVI, HDMI, Displayport) or specialized video storage (e.g. PCI Express and SATA).



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High-Performance Processing: With embedded DSP capabilities, the FPGA fabric provides unequalled parallel processing capabilities that are critical to meet the strenuous performance requirements associated with Image and Video processing. Examples include compression (MPEG-2 and MPEG-4), color space conversion, image enhancement, manipulation, scaling and recognition, among others.

Time to Market: In a market segment dominated by disruptive technologies, such as High Definition IPTV and Video on Demand, and that is still coming to terms with emerging standards, such as SMPTE424M (3G-SDI) and Dual Link-SDI (and associated source formats), to enable these disruptive technologies, it is essential that a silicon platform give aggressive companies the opportunity to develop compliant systems ahead of merchant silicon offerings. An FPGA is ideal for this purpose.

Even with these advantages, FPGAs with embedded SERDES have traditionally had formidable challenges to overcome. These challenges are in two specific areas: (a) Adapting SERDES originally architected to support Networking-based standards (Ethernet and SONET) to a specialized SMPTE HD/SD transceiver; (b) SERDES-based FPGAs command a price premium. With high-volume applications burgeoning in the market, a paradigm shift is needed in order to reduce the average selling price of the FPGAs without compromising their features and performance.

Native Multi-Rate Support on a Single Pair

SMPTE-based systems require each channel to simultaneously and dynamically support both HD and SD rates on both the Transmit and Receive channels. FPGA-

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based SERDES have traditionally been designed to provide native support for Communications and Networking-based standards. For practical reasons related to

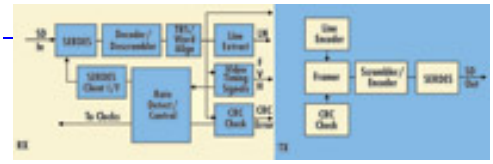
meeting performance, jitter and SERDES cost requirements, this means that most SERDES will operate over narrower frequency ranges that do not cover the entire range spanning SD (usually 270 Mb/s) and HD (1.485 Gb/s or 1.485/1.001 Gb/s) baud rates.

One way to avoid the frequency band related problems is to over-sample the low rate data by an integral factor to bring the effective data rate to the band of the higher rate data. Over-sampling for transmit is relatively straightforward, as it only requires replicating each data word a few times. Over-sampling for the receiver is a lot more challenging — the run-length (number of contiguous ‘1' or ‘0' data) of the input data gets multiplied by the over-sampling factor. The receiver Clock and Data Recovery (CDR) circuit are usually able to work with longer run-lengths of SMPTE pathological patterns (19 ones and one zero,19 zeros and one one or 20 ones and 20 zeros. This will be covered later in this article), but after over-sampling these run-lengths are multiplied by the over-sampling factor and the CDR fails to properly recover clock and data. The SERDES receiver therefore can only be used to de-serialize the data and then independently implement a parallel clock/data recovery module outside of the SERDES/PCS block. This scheme also comes with its own challenges, as it is not possible to de-serialize the serial data with respect to only the reference clock: the de-serialization is always with respect to the recovered clock, which causes the loss or mismatch of received data.

This is obviously a complex design strategy that can be avoided if a SERDES has native support for both HD and SD rates, and can handle TX and RX independently. One example of such an FPGA-based SERDES is found in the LatticeECP2M low-cost FPGA. It is also important to highlight that the networking world is largely duplex. The video world is simplex. The Rx and Tx are not generally intended to be supporting the same rate at a given time. Therefore, any FPGA transmitter and receiver would need to have rate independence built-in as a feature.

Transmit Jitter Compliance

The concept of jitter measurement for a networking-based SERDES is slightly different from that in the SMPTE world. Although timing jitter is conceptually similar, alignment jitter is unique to SMPTE.



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Timing jitter is the measure of the sinusoidal jitter amplitude over a specified frequency range relative to an ideal clock. For both HD and SD, that frequency range measures the variation in the position of signal transitions over a frequency range from 10 Hz and 148.5 MHz.

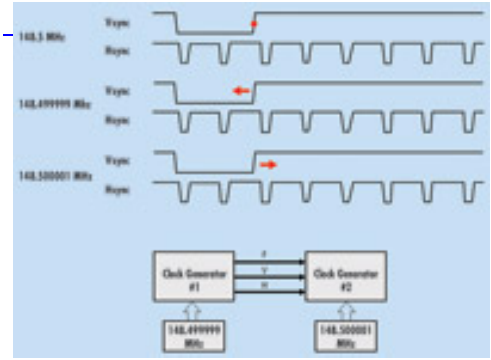
Alignment jitter, on the other hand, measures the variation in position of a signal's transitions relative to an extracted or recovered clock. In this case, the bandwidth of

the clock extraction process determines the low frequency limit for alignment jitter. The primary pattern used to measure these jitter components is the 75% Intensity Color Bar, extracted from the ubiquitous SMPTE Color Bar conceived from Al Goldberg's development at CBS Labs in the 1970s.

An FPGA with a SMPTE-capable transceiver has to be able to comply with both jitter standards, as well as the stringent parameters related to the amplitude and rise/fall times of the serial signals.

Pathological Signal Support

Special stress signals defined by SMPTE, known as pathological signals, test the ability of receivers to function properly even in worst case scenarios in an NRZ/NRZI scrambled signal environment. The main components of these signals are:



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The PLL test signal is a pathological test signal used to stress the phase-locked loop of a serial digital receiver. This is done by outputting a bit pattern which, after passing through the linear feedback shift register used to scramble serial digital signals, results (with a high degree of probability) in a long string of zeroes or ones, followed by a long string of the opposite polarity, on the digital (NRZI) signal. This can cause poorly-designed PLLs to unlock.

The Equalizer test signal consists of a long string of zeroes or ones, followed by a single bit of the opposite polarity. It can cause poorly-designed cable equalizers to malfunction.

The SDI Checkfield, standardized by SMPTE RP178 (for SD) and RP198 (for HD), is a test signal that contains one of the above signals in the upper portion of the video and the other in the lower portion of the video.

Most FPGA SERDES receivers have small capacitors (typically a few pfs) in line with recommendations provided by packet-based Networking standards. In the case of SMPTE, pathological signals have very low transition signals. Consequently, the built-in capacitor will not have the time constant to cope with infrequent charges/discharges. The result is that the average DC level falls very close to the actual signal level and can be outside the detection threshold of the receiver, causing the Clock and Data Recovery circuit to lose lock. The solution is to set the FPGA receiver in the DC coupled mode and pair it with an external capacitor.

Depending on the receiver, a capacitor in the 1 µF to 10 µF range will be able to tolerate pathological signals.

Beyond Electrical Parameters

As shown previously in Figure 1, additional logic beyond the SERDES is required to do the following:

Perform the two stage NRZ scrambling/descrambling (x^9 + x^4 + 1 polynomial) and the NRZI encoding/decoding (x + 1 equation)

Delineate aligning video words by detecting the unique 3FFh,000h,000h Timing Reference Signal (TRS)

Following the TRS decode, extract the F, V, H (Field, Vertical and Horizontal Blanking) information from the XYZ word.

In the HD standard, for the four samples immediately following the End of Active Video (EAV) packets, there is a requirement for a CRC18 field as well as the inclusion of an encoded Line Number (LN). There is no such requirement for SD; however, an optional Error Detection and Handling (EDH) module can be added.

Most importantly, a standard detector is needed to have the transceiver dynamically change between HD and SD rates. One way to do this is to program the transceiver and the external reference clock for a specific rate, and cyclically check for valid and error free video. Therefore, if no video is received, the receiver will scan for the next rate.

Ability to scale the logic to handle future standards. The rapid emergence of 3G-SDI and Dual Link-SDI demonstrates the importance of implementing the aforementioned logic in a programmable device.

Completing the Solution

Apart from the FPGA, a few other components are needed to complete the programmable transceiver solution:

(a) Multirate Reference Clock: There are many ways to implement this, including having a VCXO paired with a mux that is able to select the desired clock rate. Another alternative is a specialized video clock synthesizer that can work with a single rate oscillator (e.g. 27 MHz), and provide the required reference for SD (e.g. 270 Mb/s) and HD (e.g. 1.485 Gb/s and 1485/1.001 Gb/s). Most video processing applications require multiple video inputs and outputs. In this context, one of the most important requirements of a clock generator is its ability to Generator Lock (GenLock) the Rx and Tx video timing signals so as to synchronize both ends (shown in Figure 5). The clock chip must have the ability to take the F/V/H signals from the receiver and use them to synchronize the transmitter. Without the GenLock feature, frame buffers would need to be implemented to duplicate or drop video frames as needed. Failure to do so could result in "jumpy" images while switching between input sources.

(b) Clock Cleaner: Depending on the quality of the transmitter, as well as component and board noise, a clock cleaner with a guaranteed output jitter in the programmable loop bandwidth may be required. The clock cleaner should be positioned as close to the transceiver as possible to avoid deterministic jitter from PCB traces.

(c) Equalizer/Drivers: Video broadcast networks span many hundreds of meters: Depending on the type of 75Ω coax cable used, SD could reach a range of 300 meters and HD a range of 100 meters. An external cable driver and equalizer are therefore required. Because the cable lengths can vary, the equalizer needs to be adaptive. Users will need to budget for altered electrical parametrics when a driver is used in line with the FPGA transmitter. The driver should improve the transmit signal amplitude as well as rise and fall times. The negative impact would be in the form of additive jitter. .

Conclusion

FPGAs have arrived with a colorful bang in the Video Broadcast arena. The value of programmability that other market segments have enjoyed is now available for use in the SMPTE world. The recent advent of low-cost FPGAs equipped with high-performance transceivers and DSP blocks, like the LatticeECP2M, will make adoption even easier, and greatly reduce the build and deployment costs of video broadcast systems.

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