# Testing Challenges of SDR's

A new modeling methodology combines FPGAs and detailed circuit-level modeling in a design-to-test flow.

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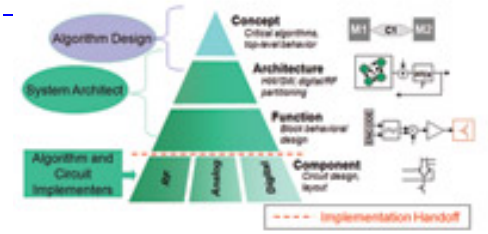


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Today's communications industry has found it essential to be able to rapidly adapt their design methodologies in order to meet their customers' ever increasing demands and expectations for more speed, range and reliability, all at a lower cost. Today, people expect to be able to communicate from anywhere, at anytime, using a wide range of technologies (e.g., WLAN, Bluetooth and Mobile *WiMAX). As the communications industry continues to grow and evolve, the ability to quickly and easily modify radio devices to support these technologies in a cost-effective manner, without requiring new hardware, will become all the more critical. Software defined radio (SDR) is one technology that promises to answer this need (see the sidebar, "Defining SDR"). Given today's rapidly evolving environment, it is essential that SDRs be modeled as completely as possible and as early as possible in the development process. Doing so minimizes risk and also helps ensure that potential problems are found early in the development process when they are easier and less costly to address, but it also shortens the development cycle and accelerates time-to-market for new products.

Simulation and modeling of SDRs should include the full mixed-domain design of the radio. Modeling of the baseband portions of the radio should not be isolated from the RF circuit level segments of the waveform path. This requires the ability to perform true mixed-domain simulations that can model the entire physical layer of the radio against key metrics, such as bit-error-rate (BER) and error-vector-magnitude (EVM), using the multiple waveforms that SDRs need to accommodate. A new methodology incorporating both FPGAs and detailed RF circuit-level modeling in a design-to-test flow now facilitates the implementation and rapid maturation of the simulated design into hardware. System performance can be verified at every step of the development process using this methodology, reducing the risk of unexpected surprises as the SDR goes from concept through to production.

**Examining Mixed-Signal Design Challenges**

While SDR today presents a host of benefits for engineers developing multi-mode, multi-band, multi-functional wireless devices, these benefits come at the cost of


new complexities and challenges which must be confronted. Many of these challenges stem from the flexibility and capabilities of FPGAs, which have become increasingly more pervasive in SDRs. The RF sections of the design must therefore be able to accommodate multiple FPGA-based waveforms. This integration of FPGA and RF circuitry adds additional complexity to an already difficult design and verification process.

Consider, for example, that the SDR's overall performance is a function of both the RF and baseband performance as well as their impairments. When determining design requirements to meet a given system-level metric such as BER or EVM, the system engineer should consider a performance budget allocation for both the RF and baseband sections. Impairments must be accounted for in the performance budget along with consideration of the different types of waveforms (e.g., OFDM, OFDMA and WCDMA, etc.) and their effects that the SDR needs to support.

Further complicating matters, the design's RF section and FPGAs may be designed by several different teams, each potentially using different tools pieced together in a disconnected design and verification flow like the one pictured in Figure 1. Quite often, the implementation phase is split between several design teams for the FPGA and RF hardware. While the FPGA design team may be writing HDL by hand for a given FGPA target, the RF design team may be performing device-level circuit simulations for the RF circuits that comprise the RF transmitter/receiver design. Because these tasks are quite different, organizational challenges often arise. Different design teams may or may not be collaborating and they may be using different tools which are not well integrated. This can introduce significant system integration risks when the FPGA and RF hardware are combined together. Design issues identified at this late stage generally require costly design re-work.

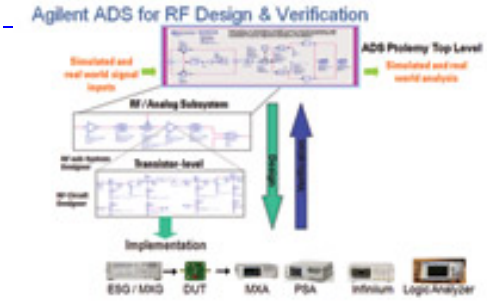
Addressing the use of disconnected tools requires a new design and verification flow that supports design team hand-offs as a design transition from algorithm to system to FPGA and RF circuit level implementation and integration. To help mitigate downstream system integration risks, the FPGA and circuit designs should also be verified together at each stage of the development process in the same simulation environment prior to hardware implementation.

**Building a Better Methodology**

A new methodology that combines the design and simulation of the FPGA and RF portions of the radio in a design-to-test flow now offer a means of overcoming the challenges of combining FPGAs and RF in the SDR (see Figure 2). At each step in the flow, the FPGA and RF designs can be verified individually or together at the component or system level, or as mixed-signal hardware. By allowing continuous system-performance verification as the different design teams evolve and refine their designs, this flow helps to minimize integration risks before the final hardware implementation.

**Algorithm Development**

At this stage, key algorithms for the FPGA-based waveform are developed and verified in simulation and as FPGA hardware. After the algorithms are developed, their performance is quickly

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evaluated to determine which ones are best suited for a given SDR application. Once a floating point algorithm is modeled, fixed-point models are introduced to evaluate their effects on the waveform fidelity. Key algorithms may be prototyped to verify functionality before assigning resources to hand-code a more optimal version for the final implementation.

As an example, consider the development of algorithms for a WiMAX IQ modulator. The advanced design system (ADS) mobile WiMAX library is used to generate IQ data which is then read into SystemVue. An algorithm design is constructed in SystemVue to up-sample and RRC filter the data and then to digitally modulate it onto a carrier. Next, HDL code is generated and exported to ADS for co-simulation with the RF design.

Once verified in simulation, the HDL code is moved into an FPGA synthesis tool for implementation onto the FPGA target. The FPGA hardware is tested using instrumentation and VSA software to demodulate the Mobile WiMAX signal.

**Transmitter Design and Circuit Co-Simulation**

The next step is to design and co-simulate the RF transmitter with the HDL code from the FPGA implementation to evaluate their combined mixed-signal performance. First, RF system components are constructed using parameterized behavioral models for blocks like amplifiers, filters and mixers. Parameters (e.g., gain, 1 dB compression point and third order intercept point) are then set for the models which can easily be adjusted and varied until the system meets the design specifications. Once defined, the parameters serve as the circuit design requirements for the system’s individual blocks. A circuit simulator is used to design

the individual RF circuits which are inserted back into the top-level system design and co-simulated to verify system performance with the circuit designs present (see Figure 3).

Continuing with the earlier example, ADS is used to co-simulate the FPGA's HDL code and RF circuit designs. ADS circuit simulators can be used to design the individual RF circuits which are then co-simulated at the system-design level. At the hardware level, ADS connects with test equipment solutions to verify the system performance with some of the designs modeled in simulation and other parts of the design available as hardware DUTs.

#### Receiver Design and Mixed-Signal Verification

In this step, the RF receiver is designed and its BER evaluated against performance impairments such as phase noise which can impact the receiver's BER/Packet Error Performance (PER) performance. BER or PER are  typically key metrics for receiver design. SDR receiver performance can also be dependent on the ADC performance with various performance attributes (e.g., the ADC's number of bits, linearity and clock jitter) impacting the receiver's ability to support different waveforms. Simulation can be used to investigate the system design sensitivity to these impairments.

It is important to evaluate the SDR receiver's performance with all the different types of waveforms that the system might have to handle. This step is useful since one of the key attributes of the SDR is its flexibility and interoperability with various waveforms. During testing and verification, it is critical to be able to quickly and easily switch between different signal types or even to present multiple different signals simultaneously that might impact the receiver's performance in a real world, high signal density environment.

Returning again to the example, the receiver design is constructed and evaluated using the ADS mobile WiMAX signal source and receiver. The ADS WiMAX source replaces HDL co-simulation to allow for more flexibility in modifying the signal waveform at the receiver input. A noise source is added to control the EbNo (SNR) at the receiver input to perform swept BER vs. EbNo simulations (see Figure 4).

Since mobile WiMAX OFDMA utilizes several different constellation types (e.g., QPSK, 16 QAM and 64 QAM), swept BER simulations are performed for each to evaluate the receiver's sensitivity to phase noise for the various constellation types. In general, the receiver's BER performance becomes more sensitive to phase noise effects as the constellation has more constellation states. Consequently, for a given EbNo and phase noise value, the receiver has better BER performance for QPSK than for 64 QAM.

Finally, a coded-BER simulation is performed on the entire system design (not just the receiver) with an IF-RF up-converter, RF transmitter design with transistor-level circuit co-simulation, signal path and RF receiver design with the ADC converters.

While the ADS WiMAX source is used for this simulation, the ADS WiMAX source could also be replaced with an HDL co-simulation block to co-simulate with the FPGA's HDL code to evaluate the mixed-signal EVM.

#### Conclusion

The increasing use of FPGAs combined with RF in SDRs has created a number of design and verification challenges. A new methodology that combines the design and simulation of the FPGAs with the RF portions of the radio offers a viable means of addressing these challenges. By evaluating their combined mixed-signal performance as the design progresses, collaboration between multiple FPGA and RF design teams can be more easily facilitated and downstream integration risks minimized. Elimination of costly design re-work stemming from identification of issues late in the design process is another key benefit.

***Note**: WiMAX is a trademark of the WiMAX Forum.

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