

# Testing LTE

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**Design simulation can be useful in addressing LTE design and verification challenges but requires consideration in selecting the appropriate model abstraction for the given phase of the design cycle.**

By Greg Jue, Agilent Technologies

Emerging standards such as 3GPP Long Term Evolution (LTE) present a number of design and verification challenges for system engineers. Some examples include determining design requirements and specifications for new hardware designs, evaluating hardware re-use, and testing RF/mixed-signal designs and hardware independently of baseband hardware.

Electronic Design Automation (EDA) simulation tools can help address these challenges by enabling system engineers to perform system-level trade-offs early in the design cycle to determine design requirements and specifications. Simulating RF and baseband designs together in one simulation environment enables evaluation of the system's RF/mixed-signal performance. Combining EDA simulation with test equipment provides flexibility in addressing testing needs for an emerging standard such as LTE. This article investigates 3GPP LTE system design and verification challenges, and shows new design simulation capabilities to help address these challenges. Several case studies highlight how design simulation can be applied to address these LTE design and verification challenges.

## Simulation Case Study - Top Level Design

A system engineer typically trades off various RF/mixed-signal requirements to make decisions on an overall performance budget allocation for a design. These trade-offs can involve baseband performance, such as the required bit-width of a fixed-point Root Raised Cosine (RRC) filter to meet a spectral mask or Error Vector Magnitude (EVM) metric. They can also involve RF performance trade-offs, such as the required transmitter LO phase noise or Power Amplifier (PA) 1 dB compression point to meet an EVM metric. The system engineer may need to trade off the required baseband performance versus RF performance to meet a system-level EVM specification.

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To illustrate this, a simplified transmitter design is constructed in EDA simulation using an LTE Uplink source, as shown in Figure 1. Parameterized behavioral models allow a top-level design to be quickly constructed and evaluated by specifying parameters such as gain, 1 dB compression point, filter order and bandwidth. Upconverter LO phase noise is specified in dBc/Hz at various frequency offsets on the LO source. The ideal Root Raised Cosine (RRC) filter in the LTE uplink signal source is replaced with a fixed-point RRC filter (inside of the hierarchical source), and the effective RRC bit-width is specified on the top level design.

The constellation types on the LTE signal source are defined as QPSK, 16QAM, or 64QAM using the LTE mapper element on the far left of the schematic. The output of the transmitter is connected to an EVM measurement sink. The simulation results at the bottom of Figure 1 show how EDA simulation can help the system engineer to trade-off RF versus baseband design requirements to meet a design performance specification such as EVM. The lower left plot shows the simulated EVM versus the RRC filter's effective swept bit-width. The middle plot shows EVM versus swept phase noise in dBc/Hz at a fixed frequency offset. The right plot shows EVM versus swept 1 dB compression point on a PA amplifier.

The system designer can trade off these baseband and RF requirements in one simulation environment to determine the top-down design requirements for the RF and baseband sections to meet a given system performance requirement such as EVM. Although time and cost are not explicitly shown, these may also be considerations in trading off the RF versus baseband performance to meet a given performance requirement.

### **Simulation Case Study - Verify System Level Performance with Detailed Baseband and RF Designs**

Design simulation can be useful in addressing LTE design and verification challenges, but requires consideration in selecting the appropriate model abstraction for the given phase of the design cycle. Specifically, models at several levels of abstraction are typically needed to support a design flow as it progresses from a conceptual phase to a detailed design phase. Top-level designs need to be quickly and easily constructed in the early design phase to evaluate system-level metrics and to perform design trade-offs.

However, improved modeling fidelity with a more detailed level of modeling abstraction is generally needed later in the design cycle to verify that the system-level performance is still being met as the development phase progresses to hardware implementation. For example, key system-level metrics, such as EVM and Bit Error Rate (BER), are evaluated on designs constructed with parameterized behavioral models which provide the high level of modeling abstraction needed to quickly construct and evaluate designs. Improved modeling fidelity is then achieved by replacing the behavioral models with HDL code or transistor-level circuit designs to verify EVM and BER as the design cycle progresses to a detailed-level design phase.

Co-simulating detailed transistor-level circuit designs together with HDL code allows the system engineer to verify the system-level performance with detailed baseband and RF designs in one simulation environment to help minimize system integration risk and unexpected surprises when system integration testing begins. Figure 2 shows an example of HDL being co-simulated together with a transistor-level circuit design in EDA design simulation to verify the system-level RF/mixed-signal performance. A fixed-point RRC is replaced with HDL code in an LTE downlink source, providing a more detailed level of baseband modeling fidelity. Similarly, the amplifier behavioral model is replaced with a transistor-level circuit design, also

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providing a detailed level of RF modeling.

The LTE downlink simulation results for the transmitter with both HDL co-simulation and circuit co-simulation are shown in Figure 3.

The LTE downlink simulation results reflect the baseband and RF simulation impairments from the RRC HDL co-simulation and RF amplifier circuit co-simulation. The constellations are shown, along with simulated EVM. The LTE downlink source allows the user to specify either QPSK, 16QAM, or 64 QAM for the User Equipment (UE).?

### Simulation Case Study - Receiver Design and Verification

Simulated EVM is shown for the transmitter design, which is typically a key metric for transmitter design performance. A key metric for receiver design performance, however, is typically Bit Error Rate (BER) or Block Error Rate (BLER).

A receiver design is constructed with parameterized behavioral models and uncoded BER curves are simulated for swept  $E_b/N_0$  into the receiver. Phase noise can be a critical issue for OFDM-based systems, so the downconverter LO phase noise was also swept for several dBc/Hz settings at a fixed frequency offset to evaluate the impact of phase noise on BER.

Figure 4 shows the simulation results for QPSK, 16QAM, and 64QAM, moving from left-to-right, respectively.

Multiple curves are shown for each case (QPSK, 16QAM, 64QAM) as a result of the LO phase noise being swept from -80 dBc/Hz to -60 dBc/Hz. Observe that the 64QAM BER performance degrades more significantly with the swept phase noise values than the QPSK BER performance as a result of the constellation states being closer to one another with 64QAM.

### Hardware Testing of R&D LTE Hardware

An emerging standard such as LTE can pose unique hardware testing challenges, and may require a flexible testing approach to address these challenges. An example is evaluating existing RF/mixed-signal hardware performance independently of the baseband section to evaluate hardware re-use for LTE. Another example is generating LTE test signals with a custom spectral mask shaped by an FIR filter. Combining the flexibility of simulation with test instrumentation can help address these testing challenges.

LTE simulation can be combined with test equipment to create and analyze physical test signals. This can be useful for component-level LTE testing, as well as system-level hardware testing (for example, uncoded BER). The test setup in Figure 5 illustrates how uncoded BER measurements can be made on a mixed-signal receiver. In this case, the DUT is not a full receiver. It is an off-the-shelf Analog-to-Digital Converter (ADC) board. However, the same approach could be used to test a mixed-signal receiver with RF inputs and digital outputs. The test setup consists of a

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signal arbitrary waveform generator, a logic analyzer, a signal source to clock the ADC board DUT and the ADC board DUT.

The EDA design simulation environment is installed inside of the logic analyzer as a custom application example. (Note, however, that the EDA solution does not ship with the logic analyzer.)

The IF input power into the mixed-signal DUT was swept from -60 dBm to -50 dBm, and the resulting uncoded BER results with an LTE downlink signal are shown in Figure 6. A 1% uncoded BER occurs at approximately -57 dBm into the DUT. Please note that this is a component-level measurement, not a sensitivity measurement for an entire receiver.

### Summary

This article discussed some design and verification challenges posed by 3GPP LTE, and showed how EDA design simulation helps address these challenges. The system design simulation case study highlighted various RF and baseband design trade-offs using metrics such as EVM and uncoded BER to evaluate the system performance. The EDA LTE design simulation functionality was then used together with instrumentation to measure the uncoded LTE BER performance of a mixed-signal DUT.

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