

# The Emergence of JESD204A in Data Converters and Low Power FPGAs in Wireless Infrastructure Equipment

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As the number of wireless subscribers skyrockets, various service types continue to proliferate, and portable access to the Internet grows more affordable, the need for increased infrastructure capacity increases daily. The advent of 3G smartphones, 3G-enabled netbooks and 3G-enabled tablet devices are major drivers in creating the explosion in demand for wireless data services and base station capacity. Performance overlays to existing wireless broadband equipment, such as HSPA+ and EV-DO (i.e., 3G+), have addressed some of these data throughput demands, but wireless service providers worldwide continue to be criticized by their customers for slow service, particularly in large metropolitan areas.

Wireless carriers have a roadmap of higher bandwidth services such as LTE and LTE-Advanced to address this challenge; however, the rollout of these 4G technologies will occur only over several years, even as data throughput requirements continue to rise. As the demand for “desk-top class” wireless broadband services becomes ubiquitous worldwide (an event industry analysts forecast will occur within the next six years), wireless service providers will be pressured to increase base station density as well. This need for a substantial increase in infrastructure equipment installations, combined with highly competitive local mar-

kets, will drive increased price pressure on base station OEMs.

## Increased Capacity with Lower Power and Cost – Myth or Reality?

Historically, higher base transceiver station (BTS) performance in the telecom industry has generally driven higher electrical power and a higher total cost of ownership. However, looking ahead, these dynamics are expected to change. Green field 3G and enhanced 3G deployments in Asia and Africa will drive relentless downward price and power consumption pressure, which very likely will ripple through the wireless infrastructure market as a whole. For wireless infrastructure OEMs, the key to maintaining and enhancing profitability lies with base station BOM cost reduction. One approach to attack BOM cost reduction has been to move from conventional, monolithic deployment of base stations to the distributed deployment model shown in Figure 1.

This topology addresses some of the challenges mentioned above, and has proliferated the use and maturity of SERDES-based logic devices to support optical data transport from the RRU (Remote Radio Unit) to the BTS. However, the remote radio units still represent a significant share of the total BTS BOM cost, due

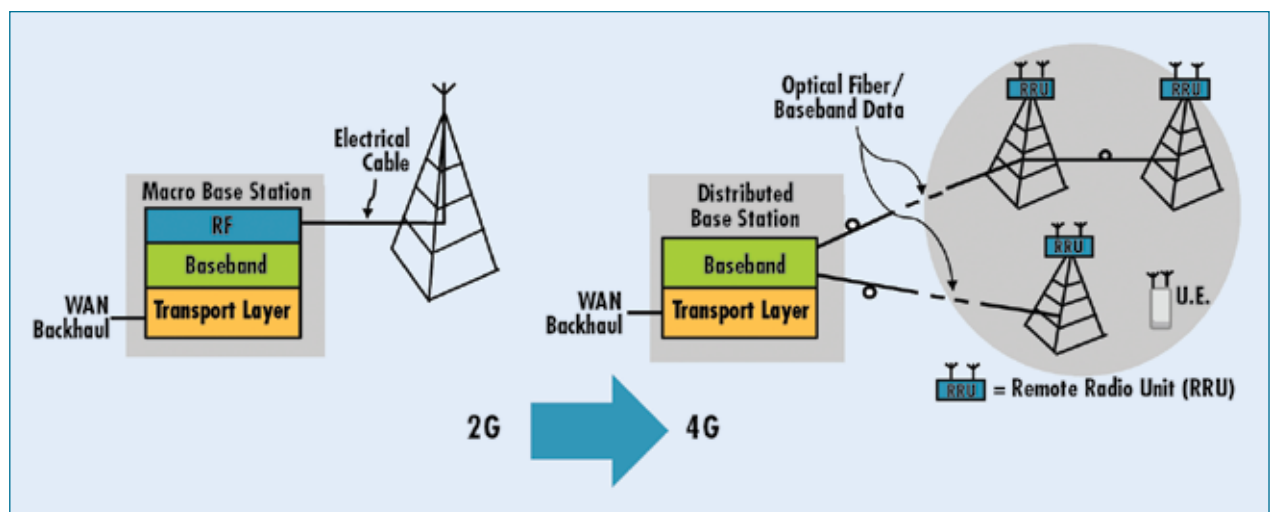


Figure 1.  
Base Station Network Evolution.

to the RF and data conversion equipment they contain. A new breed of lower cost, low power FPGAs, like the LatticeECP3 devices, have decreased overall remote radio unit costs by providing flexible data processing capabilities combined with integrated SERDES to support the CPRI and OBSAI baseband interfaces. However, increasing data throughput demands have pushed conventional parallel data converter interfaces to their limits in terms of performance, PCB layout complexity and build cost, and the efforts required to maintain data integrity. These challenges have led to the migration of the SERDES function from the BTS interface to the digital data/control interface between the actual RRU data converters and data processing FPGA(s), as shown in Figure 2. This new interface, issued by the JEDEC JC-16 committee as an open industry standard in 2008, is called JESD204A, and holds great promise for further BOM cost reduction in the remote radio unit.

The JESD204A interface, now available on CGVT™ data converters from NXP Semiconductor, is a high speed serial interface using CML-compatible differential signal levels and 8B/10B coding. The current maximum data rate is 3.125 Gbps, yielding 312.5 Mbytes/sec of bandwidth per lane, with multiple lanes between the data converter and the FPGA possible to enable arbitrary levels of system bandwidth. Because JESD204A supports precise inter-lane synchronization, it natively supports quadrature sampling, which is fundamental to the OFDM modulation scheme that underpins 3G and 4G air interfaces.

### Benefits of SERDES-based Data Converters and FPGAs

Logic programmability and high speed data conversion are technologies that have played key roles throughout the evolution of base station design. Data converters provide the bridge between the RF power amplification and RF small signal portions of the radio unit, and FPGAs provide the flexibility to allow designs to be started before an air interface specification has been completely finalized.

The increasing data throughput demands on base stations have led to increased radio unit component cost and power, with associated printed circuit board and interface complexities, as well as heightened signal integrity concerns. The BOM cost reduction and other commercial and technical merits of data conversion devices offering JESD204A compatibility are such that BTS OEMs cannot afford to overlook this new, breakthrough interface option. The technology adoption costs are quickly exceeded by

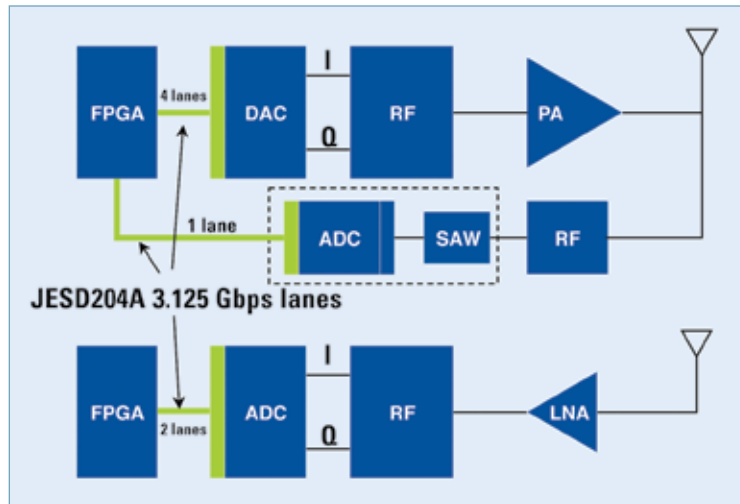


Figure 2. JESD204A Interface.

the recurring BOM cost savings, as well as the cost savings associated with improved system reliability.

JEDEC JESD204A enables remote radio unit BOM cost reduction by dramatically simplifying PCB layout, and this simplification creates the opportunity to reduce PCB layer count and PCB size, both important cost drivers. Furthermore, because JESD204A significantly reduces the number of interface signals between the data converters and FPGA(s), overall system reliability is enhanced. With the power reduction associated with low voltage swing CML, power supply BOM cost reduction is also possible. In addition to the benefits of the BOM cost reduction, JESD204A enables significant system architecture-level benefits as well. Powerful embedded protocols (with no software overhead) include data scrambling, single bit error detection and lane sync loss detection, as well as enhanced isolation between the analog and digital sections of the radio PCB, improving noise immunity. Many industry observers consider the transition of data conversion interfaces to JESD204A to be inevitable, not unlike the transition to the USB, PCI Express and Serial RapidIO high speed serial transports in the PC and DSP hardware arena.

As with data conversion devices, cost, power and performance demands have also forced FPGA architectures to undergo evolutionary changes, significantly increasing their performance, features and logic densities. The inherent flexibility and time-to-market advantages afforded by low cost FPGAs over ASICs have long been appreciated, but FPGAs traditionally have been limited to “glue logic” and “bug fix” applications. However, that is no longer the case, as the FPGA value proposi-

tion has been significantly expanded. For example, a new family of lower cost, low power FPGAs with enhanced features such as integrated SERDES, DSP datapaths and embedded memory capabilities are now available from Lattice, and have become key components in numerous remote radio unit designs. System and design engineers are now able to utilize these programmable platforms for complex signal path applications, implement-

ing functions such as Digital Down Conversion (DDC), Digital Up Conversion (DUC), Crest Factor Reduction (CFR) and Digital Pre-Distortion (DPD) at half the power and half the price of competitive SERDES-capable FPGAs.

### Summary

BTS OEMs should carefully consider the remote radio unit BOM and other cost savings enabled by the new JESD204A high speed serial interface as one important option to counter what is expected to be continued downward pressure on wireless infrastructure equipment ASPs.

FPGAs and data converters have historically played key roles in remote radio unit designs, but now they are achieving new levels of performance while helping to lower system build cost. The SERDES-based, scalable JESD204A interface provides a seamless, simplified low power and low cost data highway between the ADC/DAC(s) and the FGPA(s). Feature rich, lower cost FPGAs enable fast time-to-market and time-to-revenue, and the flexibility to accommodate evolving standards cost effectively. Systems design engineers are now equipped with an exciting, improved toolset to overcome the challenges of an ever-evolving broadband wireless marketplace. **WDD**



(Left) Ron Warner is FPGA Marketing Manager, Europe for Lattice Semiconductor Corporation. (Right) Maury Wood is High Speed Converters Product Line Manager for NXP Semiconductors.