

Software Defined Radio — the “Holy Grail” for the Industry

A new design concept is needed where the same RF design can be reconfigured to handle future radio requirements.

Software Defined Radio

The cellular device is becoming the platform for convergence; that is, all applications relating to communications, computing information, entertainment and business are getting integrated onto this platform. At the same time, hardware real estate is at a premium, and soon it will no longer be possible to continue adding new circuitry when new functions need to be included. In order to meet the requirements of future radio designs, a more flexible and upgradeable wireless platform will be necessary — enter Software Defined Radio.

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Wireless in the commercial world started in the late 1980s with the advent of car phones and 2 pound handsets that cost more than \$2000. The first problem that the industry needed to solve was that of reducing size and cost in order to make the handset a portable and mass-market device. This problem has mostly been solved; we now have phones that barely weigh a couple of ounces and cost less than \$40. The next challenge for the industry was to evolve the handset from a purely voice communications device to a multifunction device that is capable of handling data, video, music, and graphics as comfortably as voice. This requirement has also been met over the last decade by the incorporation of powerful baseband and applications and video co-processors into the hardware, along with enhanced displays and batteries. Along the way, multiple wireless protocols came into being: from the wide area standards such as EDGE, WCDMA, EVDO, and LTE to local and personal area networks such as WiFi, Bluetooth, Ultra-Wideband and NFC. In addition, as mobile phone penetration grew worldwide, new wireless frequencies have come into operation — the future handset

may have to handle seven or more different frequency bands.

New Design Concept is Needed Going Forward

At this juncture, the industry faces the next significant challenge, which is to make the wireless platform flexible, upgradeable, and future proof. The current generation of mobile devices can handle protocols and modulation formats within a protocol family such as GSM, EDGE, and UMTS and can switch from one to another through software command. They can also switch between three or four different frequency bands of operation. What’s important to note though is that these designs typically include the separate radio frequency (RF) components and circuitry for each protocol and frequency. There is obviously a problem with this kind of architectural strategy going forward. The cellular device is becoming the platform for convergence; that is, all applications relating to communications, computing, information, entertainment, and business are getting integrated onto this platform. Accordingly, hardware real estate is at a premium, and soon it will not be possible to continue adding new circuitry when new functions need to be included. What is required is a new design concept where the same RF design can be reconfigured to handle not only all of today’s radio requirements, but also future radio requirements. Another problem with

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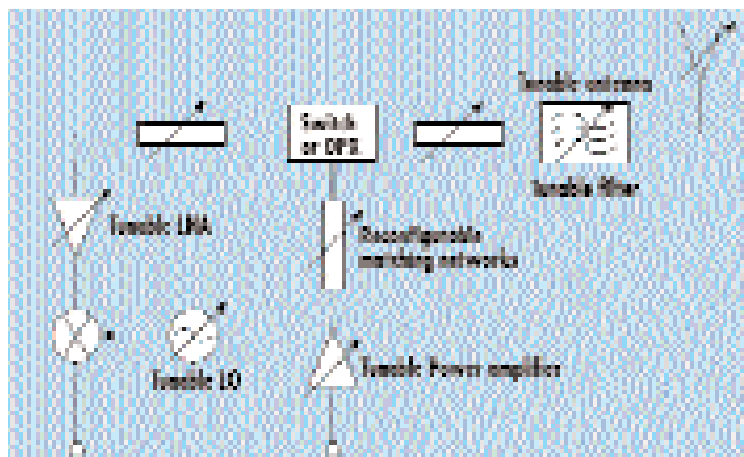


Figure 1. Wideband and adaptive RF are required for intelligent front-ends, and wideband and adaptive analog circuitry for intelligent data converters.

the traditional design approach is that high volume devices, such as mobile phones, are very cost sensitive; unfortunately, continuing to add new RF circuitry will continue to increase the total bill-of-materials. Last, the traditional approach results in hardware obsolescence. Each time a new application or service needs to be rolled out, the service provider will have to wait until a critical mass of users upgrade to the latest handset design.

Software Defined Radio — The Holy Grail

The Holy Grail for the industry is a concept termed Software Defined Radio (SDR), where the radio signal is digitized close to the antenna and then

the digital bits are manipulated completely in software, thus making the platform multiprotocol, multifunction, and multifrequency. What SDR will provide for the industry is three significant advantages: a future proof platform, a single chipset solution for the RF section of multiple product lines, and the ability to intercept market trends by offering the right product features at the right time. SDR would enable non-restrictive wireless roaming, over-the-air downloads of new features and upgrades, and reduced component costs across different product lines.

SDR's progress has been impeded by the lack of high performance RF and signal processing components. In the early years, high speed analog-to-digital (ADCs) and digital-to-analog converters (DACs) that could digitize a wideband radio signal close to the antenna either did not exist, or they consumed too much power. Second, low noise amplifiers (LNAs), variable gain amplifiers (VGAs), and filters that were tunable and adaptive did not exist in the RF domain. In addition, SDR placed considerable challenges on baseband processing, which again resulted in a lack of many practical implementations. Things are starting to change now due to a couple of reasons — the ability to implement innovative RF algorithms in CMOS technology, and the continuing advances in microelectronics, as defined by Moore's law, which is solving the power equation.

RF Front-end Design Blocks in SDR Systems

What RF front-end design blocks need to be tunable when designing a SDR system? (see Figure 1)

There are many architectural decisions to be made when implementing SDR, such as:

- For Modulation/Demodulation — Which architecture is preferable: Direct Conversion or Near-Zero intermediate frequency (IF)?
- For the ADC/DAC one has the following choices: Lowpass Delta-sigma (DS); Bandpass DS; Quadrature DS; Pipelined or Segmented/Binary.
- For the RF Sub-sampling — Should the architecture be Quadrature or Uniform Bandpass Direct Sampling?
- For the fractional-N Delta-sigma PLL Implementation — Should the design be Mixed

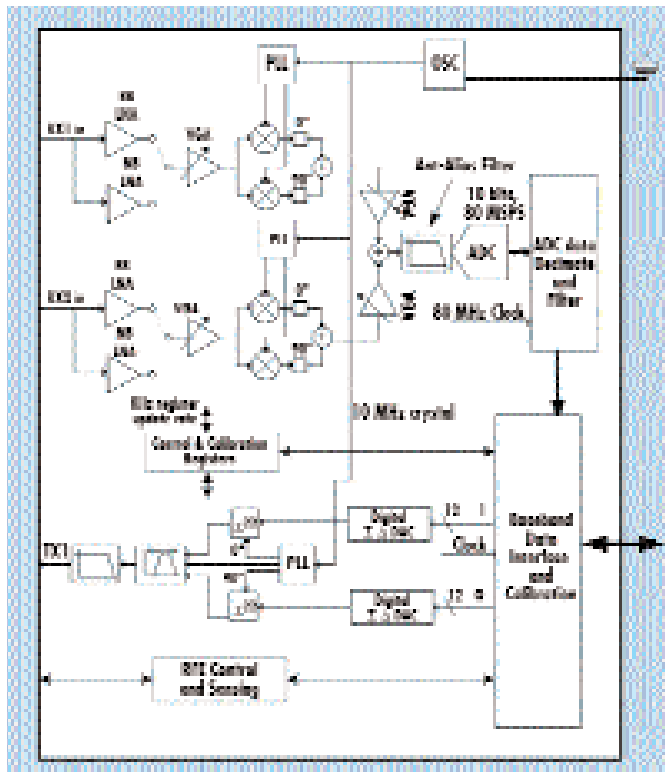


Figure 2. More specifically, tunable antennas, switchplexers, tunable matching technologies for the LNA and power amplifier, tunable filters, and ADCs/DACs using continuous-time delta modulation techniques are required in an SDR system.

- Analog/Digital or all Digital?
- For the Quadrature receiver — Should the image reject architecture be Analog or Digital? What are the Tunable-Fixed Passive RF technologies required for SDR? They are:
 - Varactor Diodes, of which there are various solutions and topologies
 - Digitally-controlled high Q capacitor arrays using MOS switches; these control the center frequency and bandwidth of the RF filter and allow high dynamic range
 - SAW, of which there are various solutions and topologies
 - BAW
 - ♦ Boundary Acoustic Wave Filters
 - ♦ Thin Film Ferroelectric Technology BST
 - ♦ MEMS, which is still not a mature technology.

Silicon Blocks in a SDR System

In a SDR system, which silicon blocks need to be tunable and reconfigurable through software command? They are the:

- LNA
- Matching Circuits
- Notch Filtering out-of-band

- Real time calibration and compensation of I/Q gain and phase errors
- Center frequency and Q of on-chip RF filters
- The ADC and DAC sampling rates
- Gain, noise figure, bandwidth, and 3rd order intercept of all the RF and analog blocks, including the data converters
- The bandwidth, Q, and order of the baseband filter
- The phase locked loop (PLL) local oscillator (LO) frequency.

Low IF and Direct RF Sampling SDR Architectures

Next, in terms of choosing between Low IF and Direct RF sampling SDR architectures, the pros and cons of each method are listed:

- Low IF sampling pros and cons

Pros

- Less DC/dynamic power*
- Lower dynamic range, low IF sampling DS ADC*
- PLL jitter has less impact on ADC Signal-to-Noise Ratio (SNR)*
- Low IF analog channelization filters*
- Lower risk design.*

Cons

- Larger die size, higher die cost*
- Individual fractional PLLs required*
- PLL has settling time requirement and phase noise concerns.*

- Direct RF sampling pros and cons

Pros

- Smaller die size, lower die cost*
- Potentially single fixed frequency integer-N PLL*
- No PLL tuning requirement.*

Cons

- Higher DC / dynamic power*
- Higher dynamic range RF sampling ADC required*
- Potential interference problems*
- Jitter has greater effect on ADC SNR*
- Channelization filtering is very difficult at RF*

Take a look at a possible practical implementation of a SDR radio that can go from 0 to 4.2 GHz (see Figure 2.)

Receiver

There are two LNAs at the front end of the receiver. The receiver can switch between narrow-band tuned LNA mode, and broad-band LNA mode, off the same input. The mode that is not selected is put to sleep. Part of the gain distribution is contained in the RF VGA. The gain range is 20 to 30 dB. This is controlled by a feedback loop from an on-chip digital signal processor (DSP). The output of the AGC feeds an image reject mixer.

The LO signals for the mixers are 90° out of phase. An additional 90° of phase shift is provided at baseband in order to sum the analog baseband signals and cancel the image frequency. The gain and phase errors for the quadrature generator are calibrated and corrected digitally using the DSP. Additional base-band AGC for each channel is provided on the order of 30 to 40 dB. The local oscill-

ator (LO) signals for the two channels are offset in frequency so that the two channels can be summed together, and combined into a single channel select and anti-alias filter followed by an ADC. The ADC is assumed to be a Pipelined ADC, but an oversampled Sigma-delta ADC can also be used. The settings for quadrature gain and phase adjust, automatic gain control (AGC), PLL, LNA program-

ming, and anti-alias filter coefficients are all controlled by digital registers.

Transmitter

The transmitter diagram in Figure 2 is a possible implementation vs. a more classical approach. A digital Sigma-delta DAC architecture is chosen. Twelve parallel channels of digitally modulated data at baseband are multiplexed into a single digital bit stream. This single bit baseband digital signal is noise-shaped; the bandwidth of the noise shaping around the center frequency is based on the oversampling ratio, as well as the order of the modulator loop. This digital bit stream is XOR-ed with the PLL-based LO, and is upconverted to a single RF digital bit stream. This stream then passes through a bandpass (BP) finite impulse response (FIR) filter, which converts the bit stream into an analog signal. The BP FIR filter consists of daisy-chained latches, with the output of each latch also driving a differential pair. The outputs of all the differential pairs are summed together, current mode, into a single load resistor. The center frequency of the BP FIR filter tracks the LO clock frequency. The RF signal then goes through an additional low pass filter which filters out transmitter harmonics and out-of-band spurs. There is AGC contained in the baseband signal. The transmitter generates the sum and difference frequencies, as well as LO feed-through in the output spectrum. By combining the I and Q outputs of the transmitter, and using innovative DSP techniques, the image and LO frequencies can be rejected by 40 to 50 dB. Additional architectural considerations are a pre-PA driver and an additional RF AGC stage to provide increased gain adjustment.

Summary

In this article we have traced the timeline of the technology inside mobile handsets, and explained why the traditional design approaches in the RF section need to change rapidly towards reconfigurable structures. The good news is that SDR architectures are starting to show up in wireless equipment and devices, and companies currently embracing SDR technology will lead the marketplace and meet their customers' future needs.

WDD

About the Author

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